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Declaration of Timothy K. Carns

Document F

E0034 CAPACITOR LOT REPORT
TDC37223

S. Girlani, M. Westphal, T. Carns and L. Debruler

March 25, 1999

Executive Summary

This report analyzes capacitor behavior from splits performed on lot E0034 (Z87L02AAR4107). The splits done on this lot were L39 IPO removal, capacitor oxide spacer, spacer etch and Pearl (325 vs. 800 Å) splits (see Table II). Each wafer received four L40 DICD splits by column. The purpose of the splits was to pinpoint which of the following leakage path was the main conduction path on SLM270 capacitor:

1. Undercut of capacitor oxide using BOE. This issue was investigated by implementing spacer oxide (RTP vs. DEP—1000 vs. 2250 Å) to seal off the void and dry/wet etch oxide. This objective was met because capacitors that received these processes showed no improvement in leakage, which indicated that undercut of oxide was not the conduction path. For confirmation, it is recommended that XSEM and hypervision be measured on wafers that have the undercut signature.

2. Pearl layer contacting both poly 1 and poly 2. This issue was resolved by not removing the oxide at L39 and by not having Pearl. Wafers that received these processes have significantly improved capacitor performance, which infers pearl as the primary conduction path. This objective was met. All of the capacitor parameters met the specification. Due to the need to use pearl for poly line-width control, split done for wafers 24 and 25 (no pearl) is not a practical process to achieve the required Leff spec. A shift in poly width (swing effect) was also observed in wafers 1 and 2 that have IPO (~375 Å) underneath pearl. This effect was not observed in wafers 7 and 15. These wafers have approximately 35 to 45 Å of oxide—grown by RTP prior to pearl deposition step. Thus, the only viable processes are wafers 7 and 15-16 (see Table II for the split list). Wafer 7 has Cpk > 1.33 for all capacitor PEVAL parameter, except CMAT.

Capacitor parameters are summarized in Table I with their spec values. Wafer 7 delivered the best overall capacitor performance with BOE for IPO removal at L39 and RTP oxidation prior to pearl deposition. Wafers 15 and 16 delivered the second best outcome with Dry etch for IPO removal at L39 and RTP. The processing splits for both wafers 7 and 15-16 are acceptable for capacitor performance. Results from these two splits are the best capacitor performance obtained so far. Further work is needed to resolve the BOE and Dry etch issue for production purpose. This issue is being addressed in E0284 lot. In any case, for an acceptable capacitor performance, it is required that pearl be isolated with a thin layer of oxide because pearl is needed for poly line-width control at L40 and it is not a dielectric.

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EFFECTIVITY: _____Immediately_____

CONTROL NUMBER

ORIGINATOR	RESPONSIBLE PERSON	DATE	DEPT #	M/S	EXT.
Suryanti Girlani	Tim Carns 3-31-99	03-12-1999	633	NB2	6912

TITLE	AFFECTED DOCUMENT	OLD REV	NEW REV
Technology Development: Z37223	TDC37223		

REASON FOR CHANGE: Add lot E0034 capacitor report

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DESCRIPTION OF CHANGE

Add attached document

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Yes No

☐ ☒ Effects process changes that modify chemical consumption and/or waste generation.

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John Smythe _____ DATE: 4-8-99

Rick White _____ DATE: 5/5/99

General Summary of Z70 Analog Capacitor Performance

T. Carns
April 02, 1999

I. Executive Summary

This report presents a summary of the current state of the capacitor technology on z372X3 and Z372x5. The objectives of this document are

1.) provide a summary of capacitor parametric data
2.) present available information on the double poly capacitor technology from other companies
3.) provide recommended specifications
4.) provide recommended process to be spec'd

The results of this report show the following capacitor process appears viable in the cap poly 2 etch block:

IPO Etch in BOE (+ resist strip) : recipe = CAPOFF
Rapid Thermal oxidation using spacer densification recipe (20 sec @ 920 C in O2) : recipe = bashful.1

The resulting parametrics for this process (lots E0034, E0417, E0033A, E0551) using the recommended specs are:

Parameter	Units	Mean	Sigma	LSL	TGT	USL	Cp	Cpk
Tox	Ang.	384.2	9.16	335	375	415	1.46	1.12
CVOLTCON	PPM/V	-11.94	5.70	-50	0	50	2.92	2.23
CVOLTCOP	PPM/V	-17.79	5.16	-50	0	50	3.23	2.08
BVOX	Volts	17.43	1.13	8	16.5	25	2.52	2.24
CMAT	%	-0.014	0.037	-0.3	0	0.3	2.73	2.60
CAPLKG@+5V	fA/um^2	0.050	0.013	-4	0	4	102.6	101.3
CAPLKG@-5V	fA/um^2	-0.119	0.075	-4	0	4	17.8	17.2
CAPLKG@+5V*	nA	0.0052	0.0013	-0.4	0	0.4	99.3	98.0
CAPLKG@-5V *	nA	-0.0123	0.0077	-0.4	0	0.4	17.3	16.8

*Leakage from SLM270 (area = 103,040 um^2).

II. Introduction

The development of the z70 double poly capacitor process has been well documented in reports contained in TDC37223 and TDC37235. The biggest problem has been with the capacitor leakage at the edge of the capacitors. This issue, in turn, resulted in degraded performance of the other capacitor parameters such as voltco and breakdown. The high leakage was found to be due to the semiconductive properties and low dielectric field strength of the PEARL layer. A number of splits have been performed to solve this issue. The most viable approach from the point of view of integrating into the current z37120 process was found in splits from lot E0034. The most successful split from that lot was one that utilized a rapid thermal oxidation (RTO) after the etching away of the capacitor oxide over poly 1 at L39. Both a plasma etch ("DRY") and BOE etch ("BOE") were investigated on that lot with the BOE split showing better results. As a result, subsequent lots were processed with this RTO (or "Cap Seal Oxide") process – some with DRY and some with BOE etch. In addition, the location of the Dry Resist Strip is also different for each of the lots. A summary of the lots and their respective IPO removal process is shown below in Table 1. A copy of the runcard pages for each lot is given for reference in Appendix A. Table 1 also shows the capacitor oxide thickness from in-fab and end-of-line electrical data. Good correlation between the mean values of the in-fab and EOL data is observed as shown in Fig. 1.

Lot#	Process	Product	Tcapox in-line	Tcapox electric	Dry Strip Location	IPO Remove
E0034#07	Z37223	Z87L02AC	364 +/- 6.2 A	376.4 +/- 2.3 A	Before IPO Remove	BOE
E0034#15,16	Z37223	Z87L02AC		374.5 +/- 2.6 A	Before IPO Remove	DRY
E0206#17,19	Z37235	Z90365BB	379 +/- 9.5 A	391.3 +/- 2.3 A	After IPO Remove	DRY
E0206#20,24	Z37235	Z90365BB		391.3 +/- 2.3 A	Before IPO Remove	DRY
E0417	Z37223	Z87L02AC	381 +/- 2.1 A	396.6 +/- 3.2 A	Before IPO Remove	BOE
E0551	Z37235	Z90233CA	374	383.5 +/- 2.9 A	None	BOE
E0033A	Z37235	Z90233CA	365 +/- 5.8 A	376.0 +/- 2.7 A	None	BOE

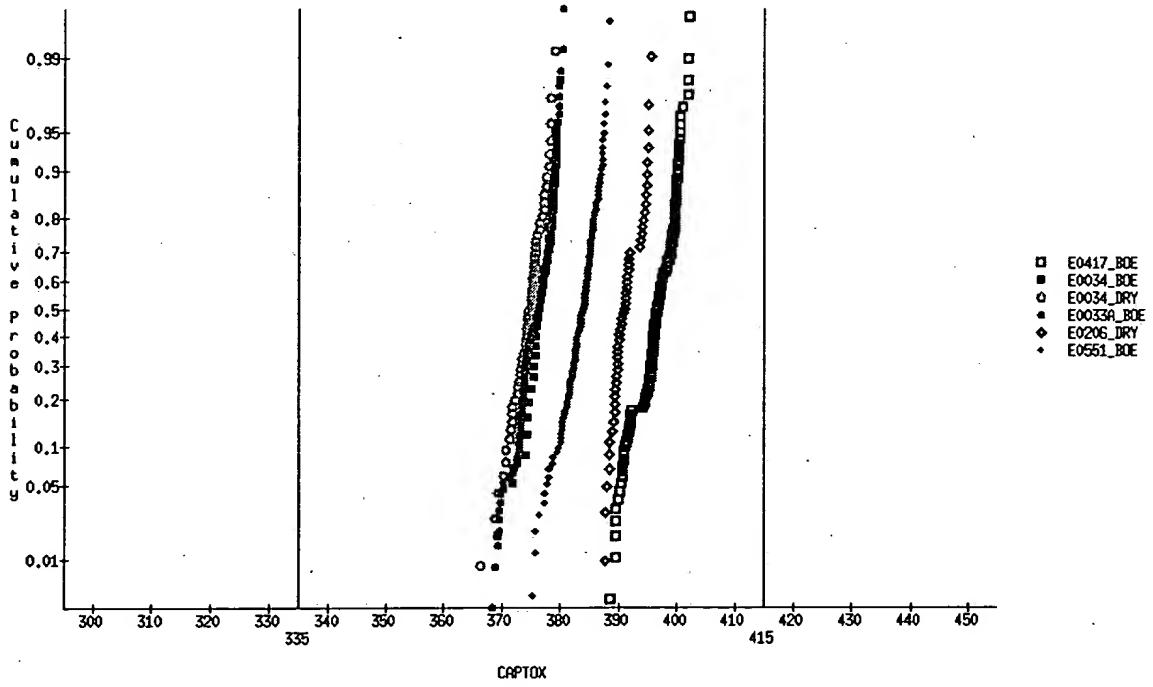
Table 1: Summary of IPO removal processing by lot. Capacitor oxide thicknesses are noted for reference.

A probability plot comparison of BOE vs. DRY etch for each capacitor parameter measured on SLM270 is shown in Figs. 3 to 9. As is apparent, the BOE process is as good or better for all capacitor parameters measured with no sites out of spec. A summary of capacitor data for the BOE process from the three lots run is given in Table 3 below. The only issue apparent at this point is the sigma for thickness. This is driven by the thicker values for E0417 as shown in Fig. 10 below. A number of lots should be run to evaluate the capacitor oxide deposition process.

Parameter	Units	Mean	Sigma	LSL	TGT	USL	Cp	Cpk
Tox	Ang.	384.2	9.16	335	375	415	1.46	1.12
CVOLTCON	PPM/V	-11.94	5.70	-50	0	50	2.92	2.23
CVOLTCOP	PPM/V	-17.79	5.16	-50	0	50	3.23	2.08
BVOX	Volts	17.43	1.13	8	16.5	25	2.52	2.24
CMAT	%	-0.014	0.037	-0.3	0	0.3	2.73	2.60
CAPLKG@+5V	fA/um^2	0.050	0.013	-4	0	4	102.6	101.3
CAPLKG@-5V	fA/um^2	-0.119	0.075	-4	0	4	17.8	17.2
CAPLKG@+5V*	nA	0.0052	0.0013	-0.4	0	0.4	99.3	98.0
CAPLKG@-5V *	nA	-0.0123	0.0077	-0.4	0	0.4	17.3	16.8

Table 3: Parametric summary of BOE with RTO with recommended electrical specification. Lots processed in this way were E0034#07, E0417 (5 wafers), E0033A (10 wafers), E0551 (7 wafers). N = 480 sites. *Leakage from SLM270 (area = 103,040 um^2).

Figure 10: Capacitor oxide thickness EOL for all lots with Cap seal oxide process.



E0417 BOE N:145 mean:396.58 std:3.2 cp:4.17 cpk:1.92
E0034 BOE N:29 mean:376.36 std:2.25 cp:5.94 cpk:5.74
E0034 DRY N:58 mean:374.53 std:2.59 cp:5.14 cpk:5.08
E0033A BOE N:180 mean:375.96 std:2.68 cp:4.97 cpk:4.86
E0206 DRY N:51 mean:391.33 std:2.33 cp:5.72 cpk:3.38
E0551 BOE N:126 mean:383.52 std:2.85 cp:4.68 cpk:3.68

VII. Conclusions and Recommendations

The results from this report show that the current double poly capacitor oxide process with BOE removal of cap oxide at L39 and the cap seal oxidation process provide a viable analog capacitor process. It is recommended that the WF3 specifications be updated to include the BOE removal and cap seal ox process. In addition, a split lot should be done to investigate the minimum and maximum allowed cap seal oxides. The minimum value is of importance for capacitor leakage considerations while the maximum oxide thickness is important due to the

potential impact on the L40 swing curve. A lot has been started (E0765) to look these issues. Finally, the PSC37223 should be updated to include the specifications recommended here as well as update the data shown.

Actions:

1. WF3 CNs to add the cap oxide BOE removal at L39 and the cap seal oxide processes.
2. Cap seal ox/PEARL margins split lot analysis (lot E0765).
3. PSC37223 CN to update data and specs.

LIST of APPENDICES

Appendix A: Capacitor Processing Runcard Pages from E0034, E0033A, E0206, E0417

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ORIGINATOR	RESPONSIBLE PERSON	DATE	DEPT #	M/S	EXT.
Tim Carns	Tim Carns 4-7-99	04/06/99	633	NB2	6944

TITLE	AFFECTED DOCUMENT	OLD REV	NEW REV
Technology Development: Z37223	TDC37223		

REASON FOR CHANGE: Add current summary of capacitor process.

☐ MAJOR

☒ MINOR

DESCRIPTION OF CHANGE

Add new document-

Summary of double poly capacitor process results and recommendations for specifications.

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Yes No

☐ ☒ Effects process changes that modify chemical consumption and/or waste generation.

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